Aufgabenblatt 11: Protokollbeschreibungen in VHDL

Auf diesem Blatt sind drei asynchrone Busprotokolle dargestellt. Ergänzen Sie die Beschreibung bzw. das Ablaufdiagramm für "'non-interlocked-"', "'half-interlocked-"' und "'fully-interlocked-"' Protokolle. (Welches Diagramm ist was?)
Berechnen Sie die gesamte Transfer-Zeit (angenommen t1=200ns, t2=300ns, t3=300ns, t4=250ns; Kanalverzögerung tk=100ns).

Aufgabe 1: _____-interlocked

Source

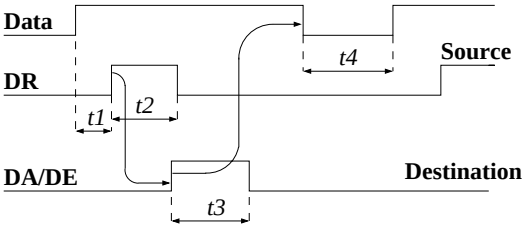
```
wait (start_tranfer'event
and start_transfer= '1');
bus_lines <= data;
DR <= '0', '1' after t1,
'0' after t2;

wait (DA'event and DA = '1')
or (DE'event and DE = '1');
RELEASE_BUS_LINES;
START_TRANSFER after t4;
```

Destination

```
wait (DR'event and DR='1');
receive_buffer <= bus_lines;
if no_error then
DA <= '1','0' after t3;
else DE <= '1','0' after t3;
end if;
```

Signalverlauf



Aufgabe 2: _____-interlocked

Source

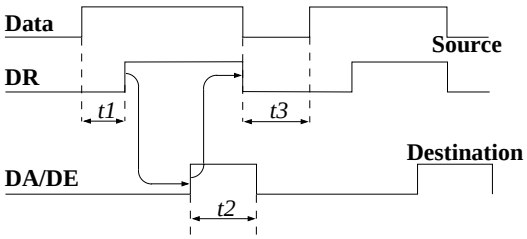
```
wait (start_tranfer'event
and start_transfer= '1');
bus_lines <= data;
DR <= '0', '1' after t1;

wait (DA'event and DA = '1')
or (DE'event and DE = '1');
RELEASE_BUS_LINES;
DR <= '0';
START_TRANSFER after t3;
```

Destination

```
wait (DR'event and DR='1');
receive_buffer <= bus_lines;
if no_error then
DA <= '1','0' after t2;
else DE <= '1','0' after t2;
end if;
```

Signalverlauf



Aufgabe 3: _____-interlocked

Source

```
wait (start_tranfer'event
and start_transfer= '1');
bus_lines <= data;
DR <= '0', '1' after t1;

wait (DA'event and DA = '1')
or (DE'event and DE = '1');
RELEASE_BUS_LINES;
DR <= '0';

wait (DA'event and DA = '0')
or (DE'event and DE = '0');
START_TRANSFER;
```

Destination

```
wait (DR'event and DR='1');
receive_buffer <= bus_lines;
if no_error then DA <= '1';
else DE <= '1';
end if;

wait (DR'event and DR = '0')
DA <= '0';
DE <= '0';
```

Signalverlauf